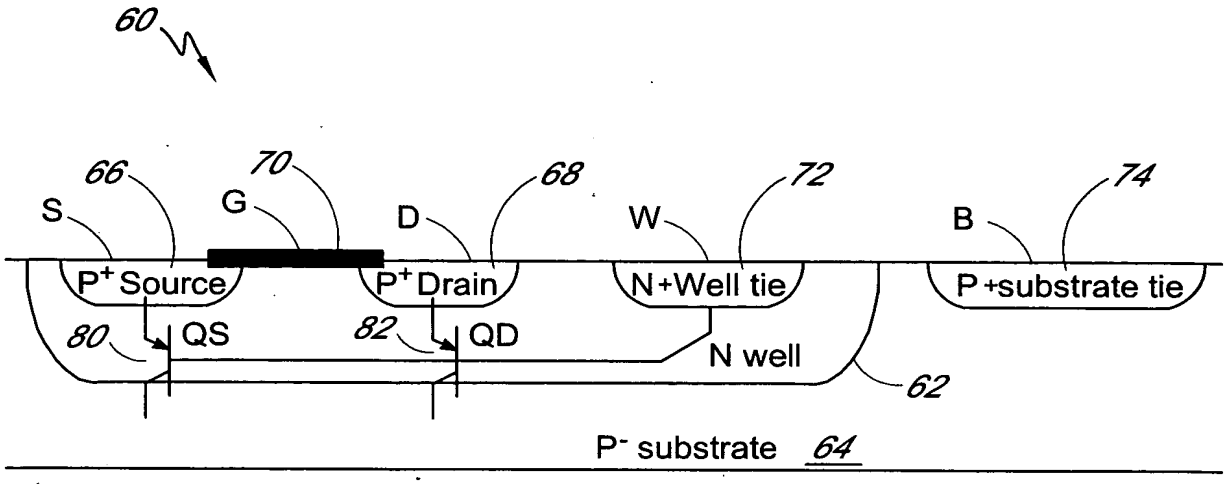
60
66
70
68
72
74
S
G
D
W
B
P+ Source
P+ Drain
N+Well tie
P+substrate tie
80
QS
82
QD
N well
62
P- substrate 64

FIG. 1

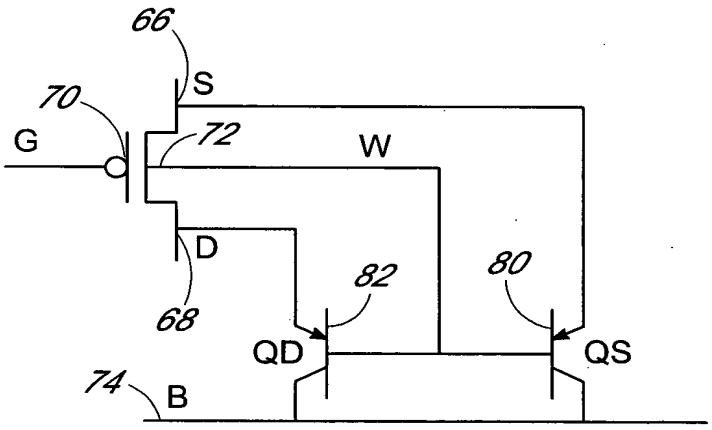
66
S
70
G
72
W
D
68
82
80
QD
QS
74
B

FIG. 2

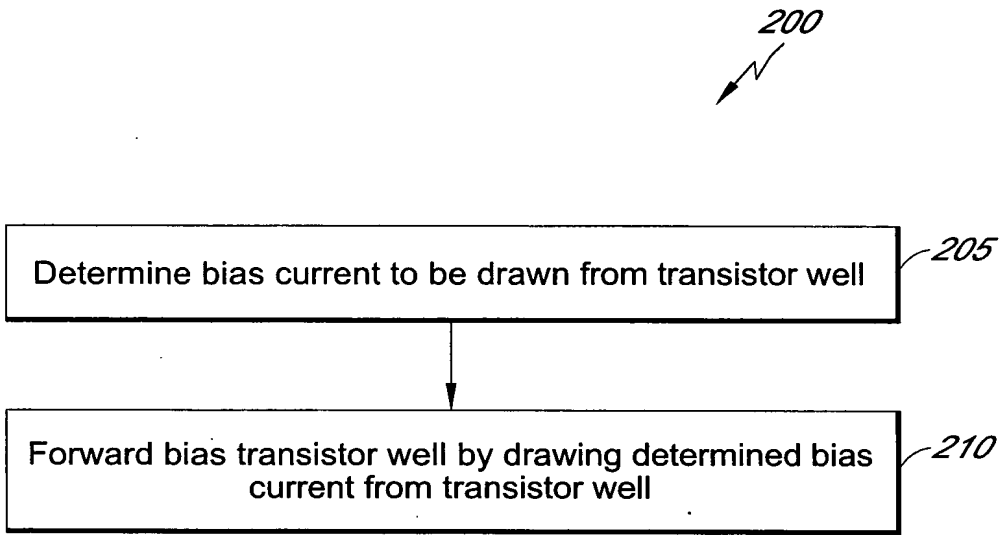
200
Determine bias current to be drawn from transistor well
205
Forward bias transistor well by drawing determined bias current from transistor well
210

FIG. 3

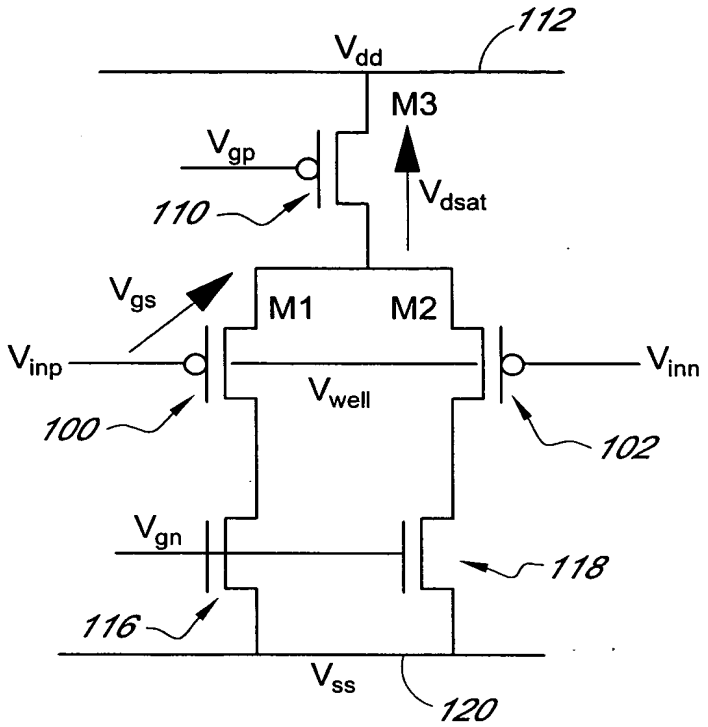
112
V_{dd}
M3
V_{gp}
V_{dsat}
110
V_{gs}
M1
M2
V_{inp}
V_{inn}
V_{well}
100
102
V_{gn}
118
116
V_{ss}
120

FIG. 4

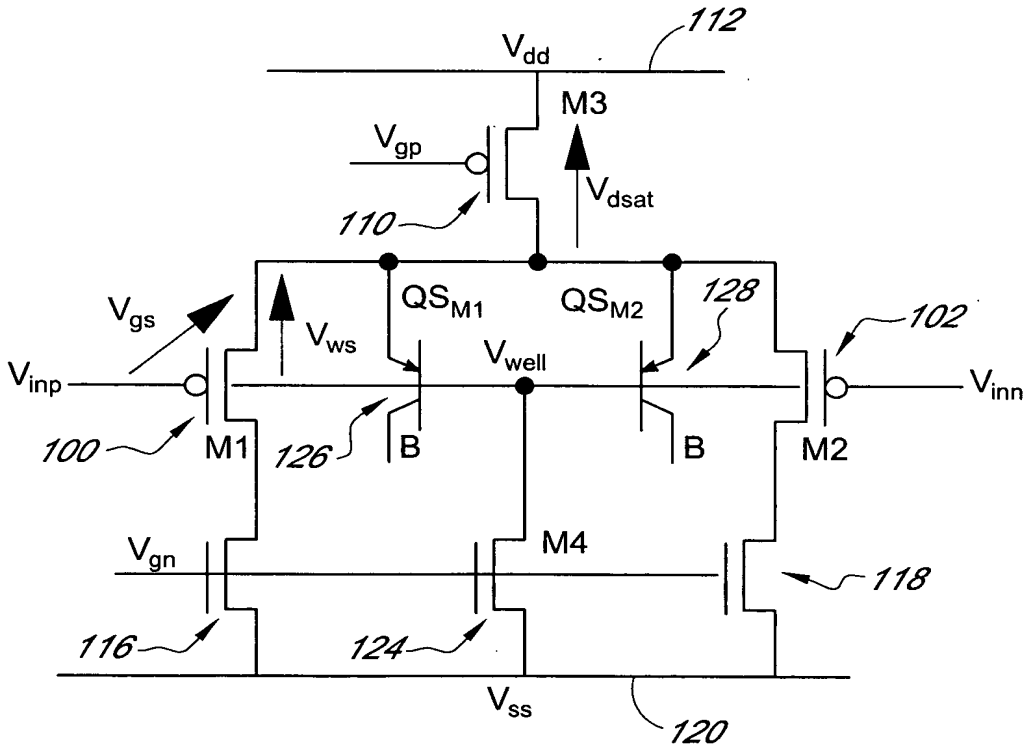
112
V_{dd}
M3
V_{gp}
V_{dsat}
110
QS_{M1}
QS_{M2}
128
102
V_{gs}
V_{ws}
V_{well}
V_{inp}
V_{inn}
100
M1
126
B
B
M2
V_{gn}
M4
118
116
124
V_{ss}
120

FIG. 5

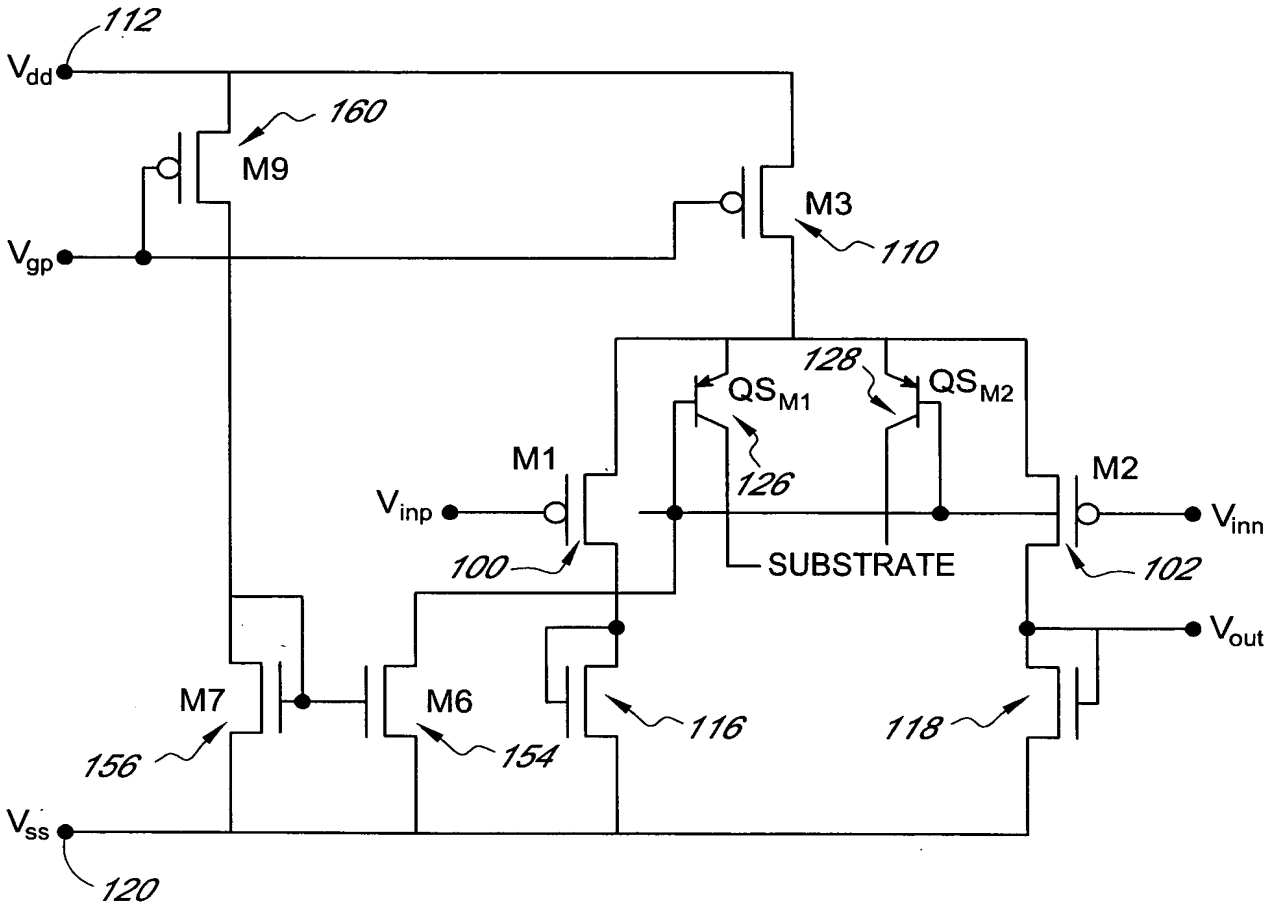
112
V_{dd}
160
M9
M3
110
V_{gp}
128
QS_{M1}
QS_{M2}
126
M1
M2
V_{inp}
V_{inn}
100
SUBSTRATE
102
V_{out}
M7
M6
116
118
156
154
V_{ss}
120

FIG. 6